Customer No.: 31561
Application No.: 10/711,677
Docket No.: 13130-US-PA

AMENDMENT

To the Claims:

1. (original) A thin film transistor array substrate having a pixel region and a peripheral region surrounding the pixel region, comprising:

a transparent substrate;

a thin film transistor array, disposed over the transparent substrate within the pixel region, wherein the thin film transistor array at least comprises a first conductive layer and a second conductive layer;

a plurality of first lead lines, disposed over the transparent substrate within the peripheral region, wherein both the first lead lines and the first conductive layer belong to a same film layer;

a plurality of second lead lines, disposed over the transparent substrate within the peripheral region, wherein both the second lead lines and the second conductive layer belong to a same film layer; and

a first shielding layer, disposed over the transparent substrate within the peripheral region to cover the gaps between neighboring first lead lines, and both the first shielding layer and the second conductive layer belong to a same film layer.

2. (original) The thin film transistor array substrate of claim 1, further comprising a second shielding layer disposed over the transparent substrate within the peripheral region to cover the gaps between neighboring second lead lines, and both the second shielding layer and the first conductive layer belong to the same film layer.

3. (original) The thin film transistor array substrate of claim 2, wherein a common

voltage is applied to the first shielding layer.

4. (original) The thin film transistor array substrate of claim 3, wherein a common voltage is applied to the second shielding layer.

5. (original) The thin film transistor array substrate of claim 1, wherein a common voltage is applied to the first shielding layer.

6. (original) The thin film transistor array substrate of claim 1, wherein the first conductive layer comprises a gate layer, and the second conductive layer comprises a source/drain layer.

7. (original) The thin film transistor array substrate of claim 1, wherein the first conductive layer comprises a source/drain layer, and the second conductive layer comprises a gate layer.

8. (original) A thin film transistor array substrate having a pixel region and a peripheral region surrounding the pixel region, comprising:

a transparent substrate;

a thin film transistor array, disposed over the transparent substrate within the pixel region, wherein the thin film transistor array at least comprises a first conductive layer and a second conductive layer;

a plurality of first lead lines, disposed over the transparent substrate within the peripheral region, wherein the first lead lines and the first conductive layer belong to a same film layer;

a plurality of first bonding pads, disposed over the transparent substrate within the peripheral region and connected to the first lead lines, wherein the first bonding pads

and the first conductive layer belongs to the same film layer;

a plurality of second lead lines, disposed on the transparent substrate within the peripheral region, wherein the second lead lines and the second conductive layer belong to a same film layer;

a plurality of second bonding pads, disposed on the transparent substrate within the peripheral region and connected to the second lead lines, wherein the second bonding pads and the second conductive layer belong to a same film layer; and

a first shielding layer, disposed on the transparent substrate within the peripheral region to cover the gaps between neighboring first lead lines, wherein the first shielding layer and the second conductive layer belong to a same film layer.

9. (original) The thin film transistor array substrate of claim 8, further comprising a second shielding layer disposed over the transparent substrate within the peripheral region to cover the gaps between neighboring second lead lines, and the second shielding layer and the first conductive layer belong to the same film layer.

10. (original) The thin film transistor array substrate of claim 9, wherein a common voltage is applied to the first shielding layer.

11. (original) The thin film transistor array substrate of claim 10, wherein a common voltage is applied to the second shielding layer.

12. (original) The thin film transistor array substrate of claim 8, wherein a common voltage is applied to the first shielding layer.

13. (original) The thin film transistor array substrate of claim 8, wherein the first conductive layer comprises a gate layer, and the second conductive layer comprises a

source/drain layer.

14. (original) The thin film transistor array substrate of claim 8, wherein the first conductive layer comprises a source/drain layer, and the second conductive layer comprises a gate layer.

15-20 (cancelled).